

Notice of References Cited	Application/Control No. 10/062,196	Applicant(s)/Patent Under Reexamination TEIG ET AL.	
	Examiner Thomas H. Stevens	Art Unit 2123	Page 1 of 1

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	C	US-6,725,439	04-2004	Homsinger et al.	716/12
	D	US-6,609,237	08-2003	Hamawaki et al.	716/10
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NON-PATENT DOCUMENTS

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	U	Papadopoulos et al., "Hierarchical Bayes Estimation for the Exponential-Multinomial Model in Reliability and Competing Risk". pg.477-484 1996.
	V	Chick-S.E., "Bayesian Analysis for Simulation Input and Output. 1997 Winter Simulation Conference. pg.253-260.
	W	Pullela et al., "Reliable Non-Zero Skew Clock Trees Using Wire Width Optimization" ACM/IEEE 1993 pg.165-170.
	X	Woodburn et al., "Computing with Uncertainty in Probabilistic Neural Networks on Silicon" May 2000. pg. 1-17.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.